Q.P. Code : 25122

First Semester B.Voc. Degree Examination,
November/December 2019

(CBCS – Freshers & Repeaters – 2017-18 and onwards)

Information Technology

Paper BVIT 102 – DIGITAL ELECTRONICS

Time : 3 Hours] *[Max. Marks : 70*

Instructions to Candidates : Answer all Sections.

SECTION – A

I. Answer any **TEN** of the following : **(10 × 2 = 20)**

1. What is positional and non-positional number system?
2. Write the rules of binary subtraction for 1's complement – method.
3. What are bidirectional shift registers?
4. Convert the following Hexadecimal to decimal:
   (a) $36F_{(16)}$ (b) $0.ABC_{(16)}$
5. Write the truth table symbol and logical expression for NOT gate.
6. What are universal gates? Give example.
7. What is the drawback of half adder circuit?
8. Define latch.
9. Expand SISO and PISO.
10. Give an example for Standard POS.
11. Write any two applications of ROM.
12. What are the basic functions in Shift Registers?

SECTION – B

II. Answer any **FIVE** questions. Each question carries **10** marks :

13. (a) Explain Demorgan's theorems. **(3)**
    (b) Apply Demorgan's theorem to the expression $(A + B)(B + C)(A + C)$. **(2)**

(c) Convert the following decimal number to binary : **(5)**

(i) 108.75

(ii) 131.5625. **(5)**

14. (a) Explain the minimization of sop expression using *k*-map method. **(5)**

(b) Simplify the Boolean expression : **(5)**

(i) $A\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}\overline{B}C$

(ii) $(x + y).(x+\overline{y}).(\overline{x}+z)$

15. Define the following terms : **(10)**

(a) Propagation delay (t_d)

(b) Set up time (t_s)

(c) Hold time (t_n)

(d) Maximum clock frequency (f_{max})

(e) Powers dissipation.

16. (a) Explain the procedure of 2's complement binary subtraction with an example. **(5)**

(b) (i) Find 2's complement of 10110010 **(5)**

(ii) Perform 110 × 111.

17. (a) Write a note on BCD Adder. **(5)**

(b) What is flip flop? Explain its types in detail. **(5)**

18. (a) Explain the working of SIPO Register. **(5)**

(b) Write a note on error correction codes. **(5)**

19. (a) Implement logic circuit using only NAND Gates $Y = \overline{A}\,\overline{B}\,\overline{C}\,D + A\overline{B}\,\overline{C}\,D + AB\overline{C}\,D + ABC\overline{D}$. **(5)**

(b) Explain the procedure of Binary division with a suitable example. **(5)**

20. (a) Explain how NOR gate can be used as universal gate. **(5)**

(b) Implement the Full ADDER circuit with Truth Table and Logical circuit. **(5)**
